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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.	
10/656,224	09/08/2003	Tzu Yu Wang	681939-15US	1061	
570 7	1590 11/14/2005		EXAMINER		
	STRAUSS HAUER	KEBEDE, BROOK			
ONE COMMERCE SQUARE 2005 MARKET STREET, SUITE 2200			ART UNIT	PAPER NUMBER	
	IIA, PA 19103		2823		

DATE MAILED: 11/14/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

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		Application No.	Applicant(s)				
Office Action Summary		10/656,224	WANG, TZU YU				
		Examiner	Art Unit				
		Brook Kebede	2823				
Period fo	The MAILING DATE of this communication app or Reply	ears on the cover sheet with the c	orrespondence address -				
WHIC - Exte after - If NC - Failu Any	ORTENED STATUTORY PERIOD FOR REPLY CHEVER IS LONGER, FROM THE MAILING DANSIONS of time may be available under the provisions of 37 CFR 1.13 SIX (6) MONTHS from the mailing date of this communication. Operiod for reply is specified above, the maximum statutory period vere to reply within the set or extended period for reply will, by statute, reply received by the Office later than three months after the mailing ed patent term adjustment. See 37 CFR 1.704(b).	ATE OF THIS COMMUNICATION 36(a). In no event, however, may a reply be tin will apply and will expire SIX (6) MONTHS from a cause the application to become ABANDONE	N. nely filed the mailing date of this communica D (35 U.S.C. § 133).				
Status							
1)⊠	Responsive to communication(s) filed on 29 Au	ugust 2005.					
	☐ This action is FINAL.2b) ☐ This action is non-final.						
3)□	3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is						
	closed in accordance with the practice under Ex parte Quayle, 1935 C.D. 11, 453 O.G. 213.						
Dispositi	ion of Claims						
4)⊠	Claim(s) 11-24 is/are pending in the application	1					
	4a) Of the above claim(s) is/are withdrawn from consideration.						
	5) Claim(s) is/are allowed.						
·	Claim(s) 11-24 is/are rejected.						
7)	Claim(s) is/are objected to.						
8)	Claim(s) are subject to restriction and/or	r election requirement.					
Applicati	on Papers						
	The specification is objected to by the Examine	r					
10) The drawing(s) filed on is/are: a) accepted or b) objected to by the Examiner.							
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).							
	Replacement drawing sheet(s) including the correcti	• , ,	• •	1(d).			
11)	The oath or declaration is objected to by the Ex	- · · · · · · · · · · · · · · · · · · ·					
Priority u	ınder 35 U.S.C. § 119		·				
12)	12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).						
a)[a) ☐ All b) ☐ Some * c) ☐ None of:						
	1. Certified copies of the priority documents have been received.						
	2. Certified copies of the priority documents have been received in Application No						
	3. Copies of the certified copies of the priority documents have been received in this National Stage						
	application from the International Bureau						
* See the attached detailed Office action for a list of the certified copies not received.							
Attachmen							
	e of References Cited (PTO-892) e of Draftsperson's Patent Drawing Review (PTO-948)	4) Interview Summary Paper No(s)/Mail Da					
3) 🔲 Inforr	nation Disclosure Statement(s) (PTO-1449 or PTO/SB/08)	5) D Notice of Informal P	atent Application (PTO-152)				
Pape	r No(s)/Mail Date	6) Other:					

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless -

- (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
- 2. Claims 11, 13, 14, 18, 19 and 22 are rejected under 35 U.S.C. 102(b) as being anticipated by Yang (US/6,159,810).

Claim Rejections - 35 USC § 103

- 3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:
 - (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.
- 4. Claims 11-24 are rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of Yang (US/6,159,810), Grider et al. (US/6,030,874) and Kim et al. (US/6,313,020).

Re claims 11, 18 and 19 Yang discloses a method for suppressing boron penetration of a gate oxide during the manufacture of an integrated circuit, comprising: providing a substrate (11 21); forming a plurality of isolation regions (20) in the substrate; forming a layer of gate oxide (13 23) over the substrate (11 21); depositing a layer of silicon material (15 25) over the layer of gate oxide (13 23); implanting ions of inert gas into the silicon layer (i.e., such as germanium ions) to create a strain between particles of the silicon layer and the implanted inert ions (i.e., to

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create amorphous region; implanting boron ions into the silicon layer to form an implanted silicon layer; patterning of the silicon layer4 and the gate oxide layer and activating the implanted boron ions; and forming source and drain regions in the substrate (see Figs. 2-12 and Col. 4, line 17 through Col. 10, line 40).

Although it is within general knowledge and level of one of ordinary skill in the art, Yang do not specifically disclose forming the gate oxide layer on the isolation regions as well as patterning of the silicon layer after boron doping process.

Grider et al. disclose method doping a silicon layer to retard from the boron diffusion into through thin gate dielectric layer the method comprises forming of a gate dielectric layer (14) on a substrate (12) and forming a silicon layer (20) on a dielectric layer and doping a silicon layer (20) with an inert ions (i.e., germanium) and doping a boron into the silicon layer after inert ions implant process performed (see Grider et al. Abstract, Fig 1-5c). In addition, Grider et al. disclose alternative process of patterning the silicon layer and the gate dielectric layer after implantation of boron ions into the inert implanted silicon layer to form pre-implanted gate pattern (see Col. 3, line 60 – Col. 4, line 2).

Both Yang and Grider et al. teachings are directed to implanting of the gate silicon layer with inert ion such as germanium ion in order to avoid boron penetration into the channel region. Therefore, the teachings of Yang and Grider et al. are analogous. Hence, one of ordinary skill in the art would have been motivated to look to analogous art teaching alternative suitable or useful methods of pattering of the doped silicon layer after implantation boron ions into inert doped silicon layer as taught Grider et al. in order to form pre-implanted gate pattern.

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Therefore, it would have been obvious to one having ordinary skill in the art at the time of applicant(s) claimed invention was made to provide Yang reference with patterning of the silicon layer after boron ion doped as taught by Grider et al. to form pre-implanted gate pattern.

Furthermore, the combination of Yang and Grider et al. do not specifically disclose the an obvious process step of forming the gate oxide layer on the isolation layer.

Kim et al. disclose forming a shallow trench isolation (STI) (15) in a substrate 10; forming gate dielectric layer (30) on the substrate (10) and on isolation (STI) (15) and forming silicon layer (60) in order to from a gate stack (see Kim et al. Fig. 6).

Yang, Grider et al. and Kim et al. teachings are directed forming a gate stack to form MOSFET device which includes ion doped silicon gate. Therefore, the teachings of Yang, Grider et al. and Kim et al. are analogous.

Therefore, it would have been obvious to one having ordinary skill in the art at the time of applicant(s) claimed invention was made to provide Yang and Grider et al. reference forming of the gate oxide layer on the isolation layer and the silicon layer on the gate oxide layer as taught by Kim et al. un order to form the gate stack consisting of the gate dielectric layer and silicon layer.

Re claim 13, as applied to claim 11 above, Yang, Grider et al. and Kim et al. disclose all the claimed limitations including the limitation wherein the plurality of isolation regions are formed by using a local oxidation of silicon process (see Figs. 2-12 and Col. 4, line 17 through Col. 10, line 40).

Re claim 14, as applied to claim 11 above, Yang, Grider et al. and Kim et al. disclose all the claimed limitations including the limitation wherein the plurality of isolation regions are

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formed by using a shallow trench isolation process (see Figs. 2-12 and Col. 4, line 17 through Col. 10, line 40).

Re claim 22, as applied to claim 18 above, Yang, Grider et al. and Kim et al. all the claimed limitations including the limitation wherein the second layer consisting of one of silicon, gallium, or a combination thereof (see Figs. 2-12 and Col. 4, line 17 through Col. 10, line 40).

Re claims 12, 16, 20 and 23, as applied to claims 11 and 18 respectively above, Yang, Grider et al. and Kim et al. all the claimed limitations including using predetermined dose of inert (i.e., such as one of helium, neon, krypton or xenon ions) and born ions. Furthermore, the claimed dose concentration range would have been optimized in order to achiever the desired device performance.

One of ordinary skill in the art would have been motivated to optimize the dopant dose range by using routine experimentation in order to achieve the claimed dopant dose range in order to achieve the desired device performance.

Therefore, it would have been to one having ordinary skill in the art at the time of the invention is made to optimize the dopant dose rant, since it has been held where the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation." See *In re Aller*, 220 F.2d 454, 456, 105 USPQ 233, 235 (CCPA 1955); *In re Hoeschele*, 406 F.2d 1403, 160 USPQ 809 (CCPA 1969); *Merck & Co. Inc. v. Biocraft Laboratories Inc.*, 874 F.2d 804, 10 USPQ2d 1843 (Fed. Cir.), cert. denied, 493 U.S. 975 (1989); *In re Kulling*, 897 F.2d 1147, 14 USPQ2d 1056 (Fed. Cir. 1990); and *In re Geisler*, 116 F.3d 1465, 43 USPQ2d 1362 (Fed. Cir. 1997). Furthermore, the specification contains no disclosure of either the critical nature of the claimed dopant dose range

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or any unexpected results arising therefrom. Where patentability is said to be based upon particular chosen dimensions or upon another variable recited in a claim, the Applicant must show that the chosen dimensions are critical. See *In re Woodruff*, 919, f.2d 1575, 1578, 16 USPQ2d, 1936 (Fed. Cir. 1990).

Re claims 15, 17, 21 and 24, as applied to claims 11 and 18 respectively above, Yang, Grider et al. and Kim et al. all the claimed limitations including using predetermined energy to produce implant ions, i.e., such as one of helium, neon, krypton or xenon ions, and born ions having predetermined density. Furthermore, the claimed implant energy range would have been optimized in order to achiever the desired implant energy.

One of ordinary skill in the art would have been motivated to optimize the implant energy range by using routine experimentation in order to achieve the claimed implant energy.

Therefore, it would have been to one having ordinary skill in the art at the time of the invention is made to optimize the dopant dose rant, since it has been held where the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation." See *In re Aller*, 220 F.2d 454, 456, 105 USPQ 233, 235 (CCPA 1955); *In re Hoeschele*, 406 F.2d 1403, 160 USPQ 809 (CCPA 1969); *Merck & Co. Inc. v. Biocraft Laboratories Inc.*, 874 F.2d 804, 10 USPQ2d 1843 (Fed. Cir.), cert. denied, 493 U.S. 975 (1989); *In re Kulling*, 897 F.2d 1147, 14 USPQ2d 1056 (Fed. Cir. 1990); and *In re Geisler*, 116 F.3d 1465, 43 USPQ2d 1362 (Fed. Cir. 1997). Furthermore, the specification contains no disclosure of either the critical nature of the claimed implant energy range or any unexpected results arising therefrom. Where patentability is said to be based upon particular chosen dimensions or upon another variable recited in a claim, the Applicant must show that the

chosen dimensions are critical. See *In re Woodruff*, 919, f.2d 1575, 1578, 16 USPQ2d, 1936 (Fed. Cir. 1990).

Response to Arguments

5. Applicant's arguments with respect to claims 11-24 have been considered but are moot in view of the new ground(s) of rejection that is necessitated by the amendment filed on August 29, 2005.

Conclusion

6. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Correspondence

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Brook Kebede whose telephone number is (571) 272-1862. The examiner can normally be reached on 8-5 Monday to Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew S. Smith can be reached on (571) 272-1907. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Brook Kebede Primary Examiner

Brook Kelede

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November 9, 2005